

Evolutionary Generation of Microwave Line-Segment Circuits by Genetic Algorithms

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Abstract—Evolutionary generation of microwave line-segment circuits is presented in this paper. Topology and dimensions of line-segment circuits are expressed by sets of parameters, which describe the way of structural growth of line-segment circuits. The sets of parameters are then optimized by genetic algorithms (GAs) to satisfy specifications. Using line segments, we can obtain not only small components for limited space applications, but also large components for wide-band frequency specifications without increasing computational complexity. In the GA process, to reduce computation time, a circuit is decomposed into lines and discontinuous elements. The S -parameters are then synthesized to obtain the response of the circuit. Three filters and a power divider are designed and tested. The results have validated our proposing procedure.

Index Terms—Filters, genetic algorithms, line segment, optimization, power dividers, topology.

I. INTRODUCTION

OPTIMIZATIONS of microwave circuits have typically been carried out for their lengths of lines by conventional methods such as the quasi-Newton method, conjugate-gradient method, or random-search technique. The initial values are obtained from conventional lumped-element prototype circuits. For complicated specifications with several passbands and stopbands, or unbalanced power-dividing ratios, we designed and optimized a circuit topology by trial and error because there were no straightforward ways to obtain initial lengths and initial topology. Therefore, we have desired a optimizing method that can treat discrete and/or discontinuous parameters such as circuit topology.

On the other hand, the genetic algorithm (GA) was introduced by Holland in 1975 [1] as a subject of computer science. Recently, however, it began to be applied to optimization problems of discrete and/or discontinuous microwave components. Michielssen applied the GA to optimizing multilayered structures such as frequency-selective surfaces in 1993 [2]. Johnson optimized antenna patterns along with the method of moment (MoM) [3]. He reduced its computation time by replacing some elements of an already-made Z -matrix of the MoM with zeros according to an antenna shape, instead of calculating the whole Z -matrix each time. Recently, these accomplishments have been compiled by Rahmat-Samii and Michielssen [4]. For analog circuits' design, Koza *et al.* synthesized linear and nonlinear circuits, combining genetic programming with SPICE [5].

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As for microwave circuit application, John and Jansen have developed an excellent way to design monolithic microwave integrated circuit or microwave integrated circuit (M)MIC components by GAs combined with a two-and-one-half-dimensional (2.5-D) spectral-domain approach (SDA) [6]. Even though this enabled them to obtain components with unconventional shapes for certain specifications, the computation time took 5 s for one component with 100 patches by a DEC alpha 200/233 because of 2.5-D SDA based on patch segments. This is good for small-size components, but not efficient for large components.

In this paper, we apply the GA to microwave circuits to optimize their topology and dimensions. Unlike the case of optimizations based on patch segments, our approach optimizing line segments does not require a large number of parameters for large circuit size. This enables us to achieve not only narrow-band specifications for small components, but also wide-band specifications for larger ones.

The GA operates on a set of parameters, therefore, circuit's topology and dimensions must be expressed by a set of parameters. The set of parameters can be optimized by the GA, even though the responses are not continuous functions of the parameters. The fact is indispensable to optimize topology of a circuit.

To reduce the computation time for evaluation of the frequency responses of many circuits, each circuit is decomposed into elements such as T-junctions, corners, and open-ends, and their S -parameters are synthesized again to obtain the responses of the circuit. For examples, in Section IV, the average computation time was approximately 3 s for 100 circuits by a PC with Celeron 400 MHz.

II. EXPRESSION OF A CIRCUIT BY A SET OF PARAMETERS

In the proposed procedure, a circuit is expressed by a set of parameters that describe structural growth of the circuit by indicating how new lines will be added to an original circuit successively. We call the original circuit a "base circuit," which is the outermost rectangular pattern. The line-adding process chooses two adjacent parallel lines in the circuit. A new line is then disposed to bridge these two lines perpendicularly. After iteration of this process, some lines are eventually removed from the circuit, as we will see later. Hereafter, we will illustrate our procedure using an example shown in Fig. 1(a)–(d).

Let a set of parameters be G as

$$G = \{ \{x_1, x_2, x_3\} \\ \{x_4, x_5, x_6, \dots, x_{3k+1}, x_{3k+2}, x_{3k+3}, \dots, x_{3N_{\max}+3}\} \\ \{x_{3N_{\max}+4}, x_{3N_{\max}+5}, \dots, x_{6N_{\max}+7}\} \}, \\ k = 1, \dots, N_{\max}. \quad (1)$$

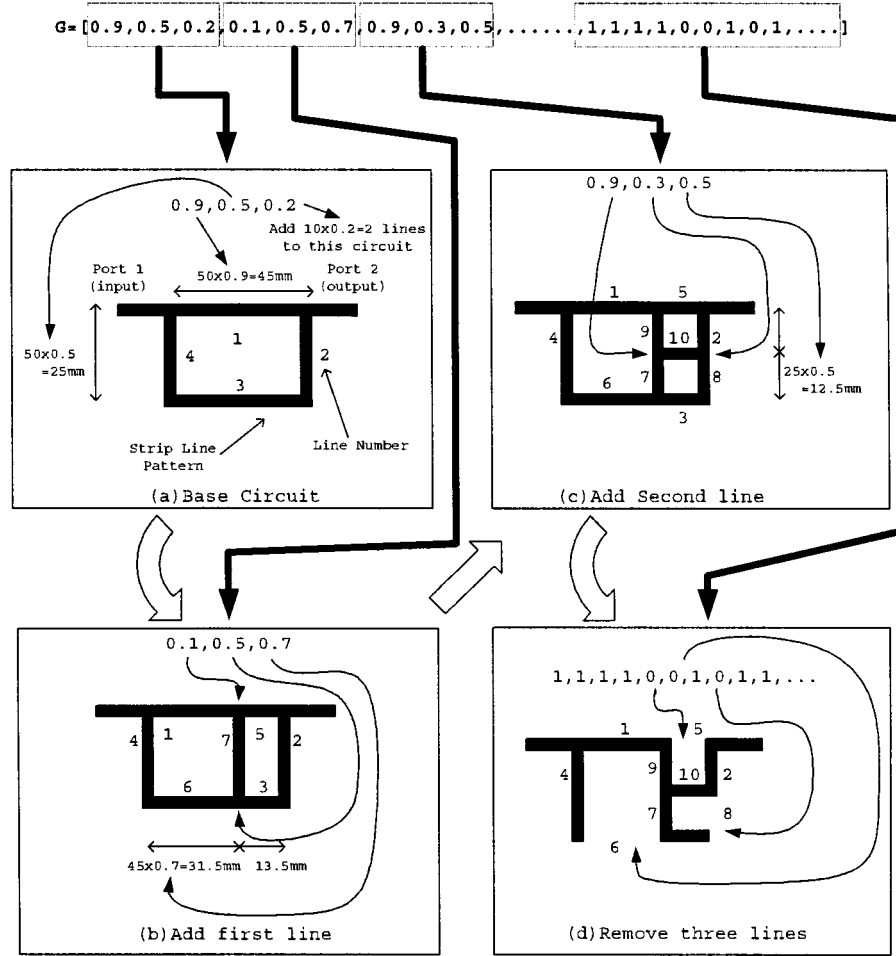


Fig. 1. Set of parameters expresses a circuit. (a) The first three parameters express the size of the circuit and the number of lines to be added. (b) Set of three parameters x_4 , x_5 , and x_6 expresses the additional first line to the base circuit. (c) Set of three parameters x_7 , x_8 , and x_9 expresses the additional second line to the previous circuit. (d) Last $3N_{\max} + 4$ parameters indicate the lines to be removed.

G is composed of three parts, i.e., the first three parameters, N_{\max} sets of three parameters, and last $3N_{\max} + 4$ parameters. Each part functions differently. Each parameter has a value between 0–1. N_{\max} specified in advance is the maximum number of lines to be added to a base circuit and this corresponds roughly to the complexity of the circuit.

In Fig. 1(a), Ports 1 and 2 are the input and output ports. This circuit consists of distributed lines of the same width. The first two parameters x_1 and x_2 define the x and y dimensions of a base circuit. The third parameter x_3 defines the number of lines to be added to the base circuit. If X_{\max} and Y_{\max} are the maximum x dimension and the maximum y dimension of the circuit, then the actual x and y dimensions are $X_{\max} \cdot x_1$ and $Y_{\max} \cdot x_2$ as shown. Note that the dimensions are not larger than $X_{\max} \times Y_{\max}$ because x_1 and x_2 are less than one. Thus, X_{\max} and Y_{\max} are considered as scaling factors that we can tune for each problem. The number $N_{\max} \cdot x_3$ indicates how many lines will be added to a base circuit up to N_{\max} . In this example, we specified $N_{\max} = 10$, which indicates two lines would be added because $N_{\max} \cdot x_3 = 10 \cdot 0.2 = 2$.

The N_{\max} sets of three parameters of x_{3k+1} , x_{3k+2} , and x_{3k+3} , where $k = 1, \dots, N_{\max}$ indicate how the k th line is added to the base circuit successively. This procedure is explained in Fig. 1(b) and (c).

The stage of $k = 1$ corresponds to the operation to choose the first line to be added to the base circuit. Note that the total number of lines in the base circuit is four. The process chooses one line out of the four existing lines as a starting point of a new line, according to x_4

$$\begin{aligned} \text{line 1 is chosen if } 0 \leq x_4 < \frac{1}{4} \\ \text{line 2 is chosen if } \frac{1}{4} \leq x_4 < \frac{2}{4} \\ \text{line 3 is chosen if } \frac{2}{4} \leq x_4 < \frac{3}{4} \\ \text{line 4 is chosen if } \frac{3}{4} \leq x_4 \leq 1. \end{aligned} \quad (2)$$

In the case of $x_4 = 0.1$, line 1 is chosen, and we call this line the “starting line.”

Choose another line out of the lines facing the starting line according to x_5 , i.e., x_{3k+2} , when $k = 1$. The meaning of “facing” is that we can make a vertical or horizontal line from the starting line to the chosen line. In this case, such a line is only line 3 as follows:

$$\text{line 3 is chosen if } 0 \leq x_5 \leq 1. \quad (3)$$

We call this line the “ending line.”

x_6 indicates the position of the new line. In this example, the y position of one end of the new line must be the same as that of line 1 and the other end of the new line must be the same as that of line 3. Therefore, the x position remains to be determined by x_6 . If the leftmost possible position of the line is $x = 0$ and the rightmost possible position is $x = X_{\max} \cdot x_1$, x_6 indicates a point between them. The x position of the new line is

$$x_{\text{new line}} = (X_{\max} \cdot x_1 - 0) \cdot x_6. \quad (4)$$

The total number of lines increases by three because the starting and ending lines have been divided into two parts, as shown in Fig. 1(b) (i.e., Line 1 \rightarrow Line 1 + Line 5 and Line 3 \rightarrow Line 3 + Line 6). This process of the first line ends up by renumbering the lines this way.

We then go to the next stage to add the second line to the previous circuit. Repeating the same procedure, we choose one line out of the seven lines, according to x_7 , i.e., x_{3k+1} when $k = 2$

$$\begin{aligned} \text{line 1 is chosen if } 0 \leq x_7 < \frac{1}{7} \\ \text{line 2 is chosen if } \frac{1}{7} \leq x_7 < \frac{2}{7} \\ &\vdots \\ \text{line 7 is chosen if } \frac{6}{7} \leq x_7 \leq 1. \end{aligned} \quad (5)$$

In the case of $x_7 = 0.9$, line 7 is chosen as the “starting line.” For the “ending line,” we choose one line from the two possible lines, i.e., lines 2 and 4, as follows:

$$\begin{aligned} \text{line 2 is chosen if } 0 \leq x_8 < \frac{1}{2} \\ \text{line 4 is chosen if } \frac{1}{2} \leq x_8 \leq 1. \end{aligned} \quad (6)$$

The total number of the lines becomes ten. The circuit pattern is shown in Fig. 1(c). In this example, the line-adding process ends when we add two lines because $N_{\max} \cdot x_3 = 2$.

If we need to add a k th line, repeating the same procedure, we choose one line out of the $4 + 3(k - 1)$ lines according to x_{3k+1} as follows:

$$\begin{aligned} \text{line 1 is chosen if } 0 \leq x_{3k+1} < \frac{1}{3k+1} \\ \text{line 2 is chosen if } \frac{1}{3k+1} \leq x_{3k+1} < \frac{2}{3k+1} \\ &\vdots \\ \text{line } 3k+1 \text{ is chosen if } \frac{3k}{3k+1} \leq x_{3k+1} \leq 1. \end{aligned} \quad (7)$$

For the “ending line,” we choose one line from the lines facing the starting line that are not always one or two, but always less than $3k$. The x position or the y position is determined the same way as mentioned above. We repeat the process $N_{\max} \cdot x_3$ times and finally get $3N_{\max} \cdot x_3 + 4$ lines in the circuit.

The last stage removes some lines out of the $3N_{\max} \cdot x_3 + 4$ lines. The first $3N_{\max} \cdot x_3 + 4$ parameters of the last $3 \cdot N_{\max} + 4$ parameters of G are corresponding to the lines in the circuit and have values of zero or one. Other parameters of the last set are not used. If the value is zero, the corresponding line is

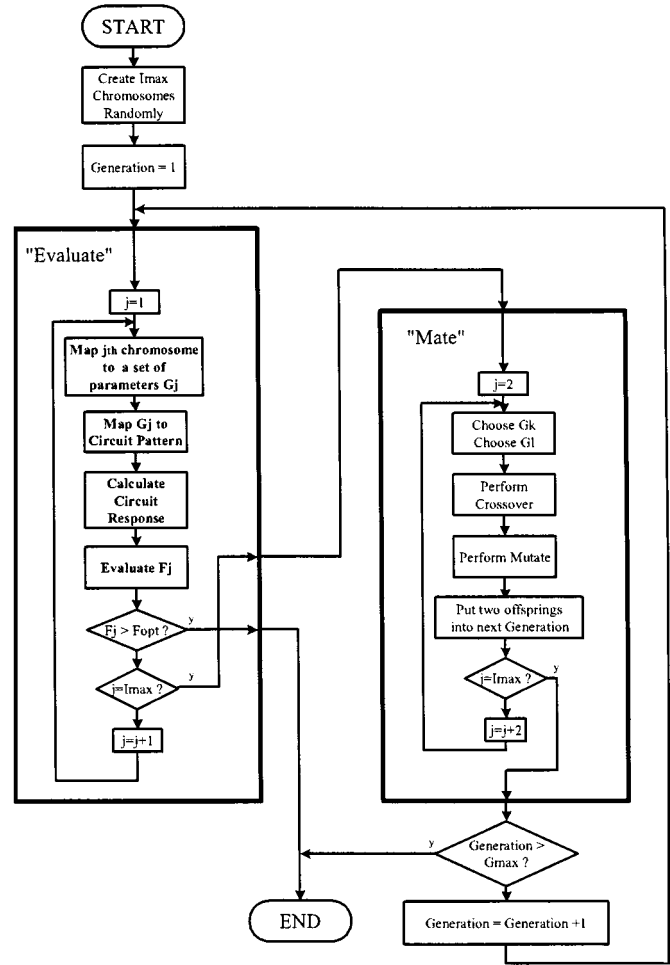


Fig. 2. GA flowchart. The GA consists of two main part, i.e., “Mate” and “Evaluate.”

removed from the circuit. If the value is one, the corresponding line remains. The case that lines 5, 6, and 8 are removed from Fig. 1(c) is shown in Fig. 1(d).

The proposed procedure has the following features.

- 1) The circuit may have loops and then may have a frequency response utilizing phase interference effect by different signal routes, in which low insertion loss is expected because of its nonresonance mechanism.
- 2) The fact that any set of arbitrary parameters corresponds to a certain feasible circuit avoids creation of a meaningless set of parameters that generates an infeasible circuit. Increasing of the number of such sets hinders convergence of the GA.
- 3) The fact that circuit size is not restricted by the number of parameters, but only by X_{\max} and Y_{\max} enables us to apply the procedure to a large circuit for wide-band specifications, as well as a small component for limited space specifications.

III. OPTIMIZATION BY THE GA

The flowchart of the proposed GA is shown in Fig. 2. The algorithm consists of two parts, namely, “Mate” and “Evaluate”

TABLE I
GA TERMINOLOGY

Chromosome	sequence of binary numbers, which are decoded into real parameters
Gene	binary number composing a chromosome
Population	number of chromosomes in one generation
Parent	chosen chromosome to create children
Child	chromosome created from a couple of parents
Generation	iteration stage where GA creates children as much as a certain population
Fitness	certain value indicating how the response of a chromosome is close to the goal
Crossover	GA operation exchanging some genes between two chromosomes
Mutation	GA operation flipping some genes as “0” to “1” or “1” to “0”

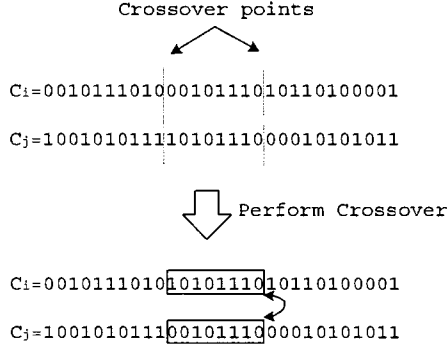


Fig. 3. Crossover exchange parts of chromosomes between parents.

procedures. “Mate” is a common procedure of the GA and “Evaluate” must be developed for each application. We will give a brief explanation for “Mate” as the common procedure and then go to our “Evaluate” procedure. Further explanations for “Mate” can be found in [4], and the typical GA terminology is carried in Table I.

A. “Mate” Procedure

“Mate” creates new chromosomes that we call “children” into the next generation. In each generation, the GA chooses chromosomes as parents depending upon their fitness. The chromosome that has high fitness would be chosen frequently, but the one that has low fitness fails to be chosen. Let the fitness of chromosome j be F_j . The probability for chromosome j to be chosen is then defined as

$$\text{Probability of } j = \frac{F_j}{\sum_{k=1}^{I_{\max}} F_k} \quad (8)$$

where I_{\max} is the population. The way to calculate fitness is described in Section III-B.

“Crossover” is performed when two children are created. Let the two chosen chromosomes be C_i and C_j , as shown in Fig. 3. A pair of crossover points is set randomly. The binary numbers between them are then exchanged. The two different created chromosomes inherit some features of their parents. This is why we call them “children.”

“Mutate” is performed on the created child. Some mutation points are set randomly for each chromosome. Genes at the points are flipped, as shown in Fig. 4. The created chromosomes are expected to have different characteristics from the original ones. This causes the divergence of a variety of circuit patterns.

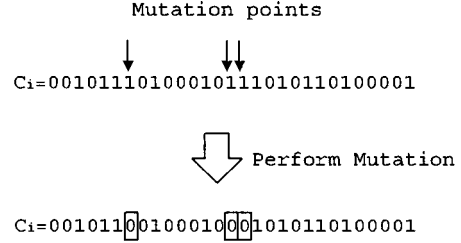


Fig. 4. Mutate flips of some genes in chromosomes of children.

After these two new children are put into the next generation, the two parents are taken back to the original set and the GA repeats the same procedure until the number of children of the next generation becomes I_{\max} . The outer loop controls iteration of generations. G_{\max} is the limit of this iteration.

B. “Evaluate” Procedure

We will explain each “Evaluate” procedure in Fig. 2 using Fig. 5. “Map j th chromosome C_j to a set of parameters G_j ” translates a sequences of binary numbers in Fig. 5(a) to a set of parameters of real numbers in Fig. 5(b), following a rule defined in advance.

“Map G_j to circuit pattern,” which corresponds to Fig. 5(c), creates physical circuit patterns from sets of parameters, with the procedure developed in Section II. “Calculate circuit response,” which corresponds to Fig. 5(d), calculates responses of circuits by composing their S -parameters from T-junctions, corners, open-ends, and uniform transmission lines. We construct the scattering matrix \mathbf{S} that includes all the elements appearing in the circuit pattern and the connection matrix $\mathbf{\Gamma}$. The element T_{ij} of the matrix T defined as

$$\mathbf{T} = (\mathbf{\Gamma} - \mathbf{S})^{-1} \quad (9)$$

is the response at node i with an incidence at node j . In the case that node 1 corresponds to the input port and node 2 corresponds to the output port, T_{11} represents the reflection coefficient and T_{21} represents the transfer coefficient [7], [8].

“Evaluate F_j ,” which corresponds to Fig. 5(e), evaluates the fitness of each response of the circuit by a specific function. When $F_j = F_{\text{opt}}$, where F_{opt} is the optimal value of the fitness, the chromosome meets all the specifications. The definition of the probability and (8) restrict the fitness to a positive value.

For designing a filter, the specifications are $S_{11}[\text{dB}] < V_1[\text{dB}]$ in passbands and $S_{21}[\text{dB}] < V_2[\text{dB}]$ in stopbands,

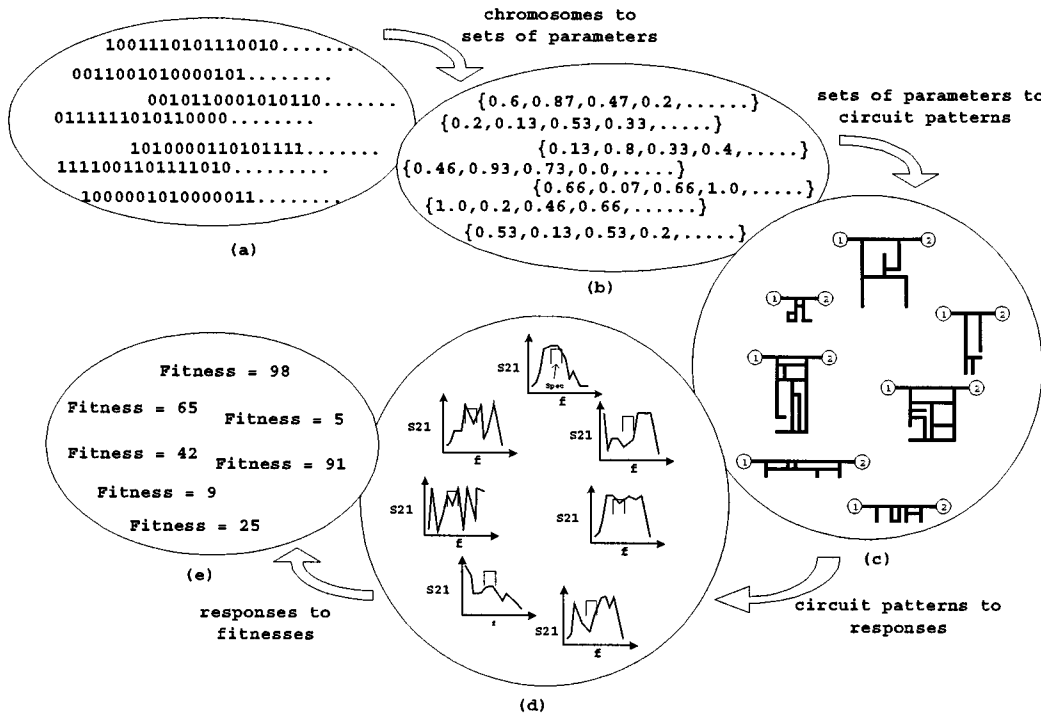


Fig. 5. Evaluate procedure operates on five states of: (a) chromosomes, (b) sets of parameters, (c) circuit patterns, (d) responses, and (e) fitnesses.

where V_1 and V_2 are specified S -parameters in decibels. We define the fitness as

$$\text{fitness} = \sum_n \left\{ \min [-V_{c,n}, -V_{e,n}] \times W_n \right\} \quad (10)$$

where $V_{c,n}$ is the S -parameter of the circuit at the n th sampling frequency in decibels, $V_{e,n}$ is the expected S -parameter at the same frequency in decibels, and W_n is a weighting value. The “-” signs are due to the fact an S -parameter of a passive element is negative in decibels.

For another example of designing a power divider, we specify that

$$\begin{aligned} S_{21}[\text{dB}] &< V_3[\text{dB}] \\ S_{31}[\text{dB}] &< V_4[\text{dB}] \\ S_{32}[\text{dB}] &< V_5[\text{dB}] \\ S_{11}[\text{dB}] &< V_6[\text{dB}] \\ S_{22}[\text{dB}] &< V_7[\text{dB}] \\ S_{33}[\text{dB}] &< V_8[\text{dB}] \end{aligned} \quad (11)$$

where V_3 to V_8 are specified S -parameters in decibels. We define the fitness as

fitness

$$\begin{aligned} &= \sum_{S_{21}, S_{31}, S_{32}} \left\{ \sum_n \left\{ (-V_{e,n} - \min [-V_{e,n}, |V_{e,n} - V_{c,n}|]) \right. \right. \\ &\quad \left. \left. \times W_n \right\} \right\} \\ &+ \sum_{S_{11}, S_{22}, S_{33}} \left\{ \sum_n \left\{ \min [-V_{c,n}, -V_{e,n}] \times W_n \right\} \right\}. \end{aligned} \quad (12)$$

IV. DESIGN EXAMPLES

Several harmonic stripline filters passing f_0 and stopping $2f_0$ and $3f_0$ are designed, fabricated, and tested. In all examples, $X_{\max} = Y_{\max} = 50$ mm and $N_{\max} = 8$. The CPU used was Celeron 400 MHz.

A traditional four-stage low-pass filter with a response of passing below 2.1 GHz and stopping above 3.8 GHz was fabricated for comparison. A final circuit pattern was obtained by a conventional optimization by MDS.¹ The size was 21.8×7.6 mm² and the wavelength was 87.5 mm at 2 GHz on the substrate whose permittivity was 2.94 and thickness was 1.0 mm. The circuit pattern and frequency responses are shown in Fig. 6(a) and (b). The inverted small triangles indicate the specifications of the harmonic filter. The specifications are barely met. The insertion loss was 0.50 dB at 2 GHz.

Fig. 7(a) shows the circuit pattern of a harmonic filter by the GA in the same stripline structure and Fig. 7(b) is its frequency responses. The specifications are $S_{11} < -15$ dB from 1.9 to 2.1 GHz and $S_{21} < -15$ dB from 3.8 to 4.2 and 5.7 to 6.3 GHz. The size of the filter was 13.1×11.5 mm², which was 10% smaller than the traditional one. All specifications were met in this example. The insertion loss was 0.52 dB at 2 GHz. The computation time was about 5 h with 500 chromosomes.

Figs. 8(a) and (b) and 9 show another example with an additional stopband below the passband, which was $S_{21} < -15$ dB from 1.4 to 1.5 GHz. The other specifications were $S_{11} < -15$ dB from 1.95 to 2.05 GHz and $S_{21} < -15$ dB from 3.9 to 4.1 and 5.85 to 6.15 GHz. The size was 46.8×35.4 mm². The thin lines in Fig. 8(b) are the responses of the calculation. Measured responses were shifting 100 MHz higher at 4 GHz and 200 MHz at 6 GHz. This was

¹Agilent Technol. MDS B7.20, Santa Clara, CA.

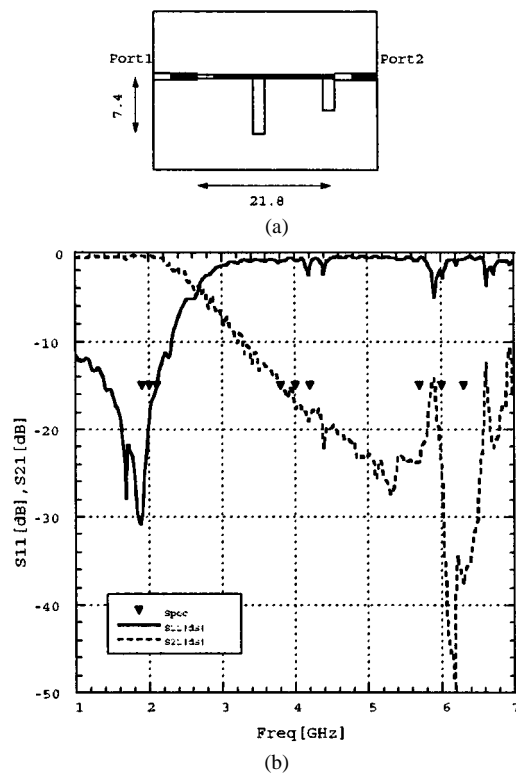


Fig. 6. Fabricated traditional four-stage low-pass filter. The passband is below 2.1 GHz and the stopband is above 3.8 GHz. (a) Pattern. (b) Responses.

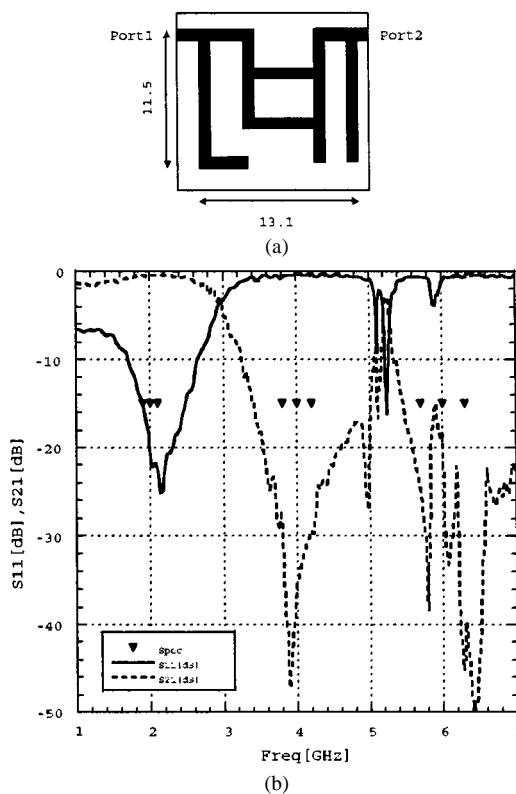


Fig. 7. Fabricated four-stage low-pass GA filter. The passband is from 1.9 to 2.1 GHz and stopbands are from 3.8 to 4.2 and 5.7 to 6.3 GHz. (a) Pattern. (b) Responses.

caused by the air region around the stripline conductor. The region decreases the effective permittivity. The computation

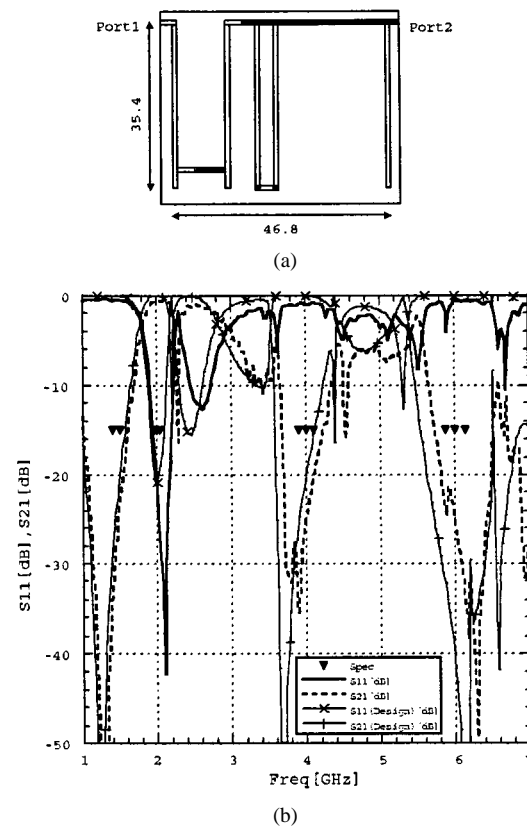


Fig. 8. Fabricated four-stage low-pass GA filter with one stopband below the passband. The passband is from 1.95 to 2.05 GHz and stopbands are from 1.4 to 1.5, 3.9 to 4.1, and 5.85 to 6.15 GHz. (a) Pattern. (b) Responses.

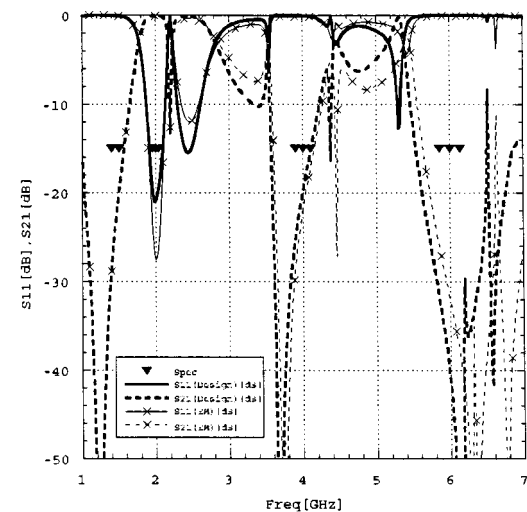


Fig. 9. Comparison of results of GA design and responses by full wave EM simulation for Fig. 8(a).

time was approximately 14 h. Fig. 9 shows the responses of our calculation and the responses of the full-wave electromagnetic (EM) simulation EMSight.²

Fig. 10(a) and (b) shows another example of more challenging specifications. At 3.5 and 5.5 GHz, S_{11} was specified below -15 dB. At 2.5 and 4.5 GHz, S_{21} was specified below -15 dB. Each bandwidth was 0.2 GHz. The size was

²AWR Microwave Office 2001, ver. 4.01, El Segundo, CA.

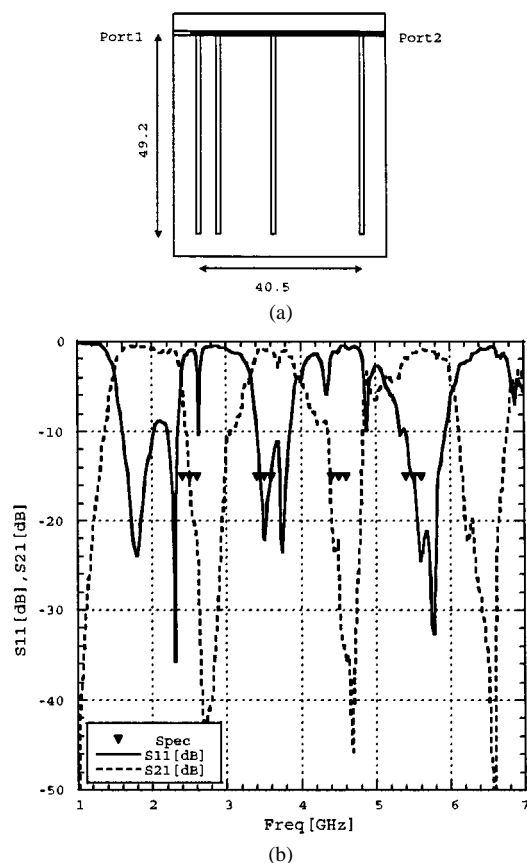


Fig. 10. Fabricated GA filter with two passbands and two stopbands alternatively. Passbands are from 3.4 to 3.6 and 5.4 to 5.6 GHz and stopbands are from 2.4 to 2.6 and 4.4 to 4.6 GHz. (a) Pattern. (b) Responses.

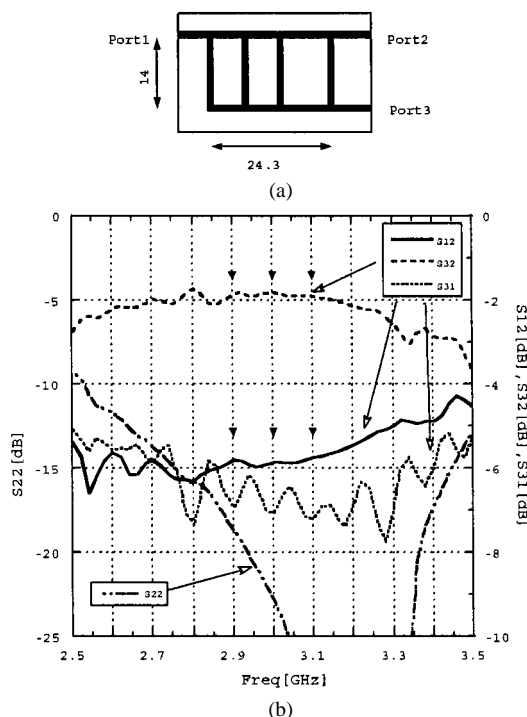


Fig. 11. Fabricated GA power divider. Power from ports 2 to 1 is 30% and that from ports 2 to 3 is 70%. (a) Pattern. (b) Responses.

$40.5 \times 49.2 \text{ mm}^2$. The frequency-response shift to higher frequency again and some specifications were not met in its lower

edge of the frequency bands. The computation time was approximately 10 h.

Fig. 11(a) and (b) shows an example of a power divider when port 2 was the input terminal. From 2.9 to 3.1 GHz, S_{12} was specified at -5.23 dB within an error of 0.3 dB , and S_{32} was specified at -1.55 dB within an error of 0.15 dB . This means the input power from port 2 is divided into 30% at port 1 and 70% at port 3. S_{22} was also specified below -15 dB . The size was $24.3 \times 14 \text{ mm}^2$. The computation time was 30 min. In this case, the isolation was not specified, therefore, it was not very good.

V. CONCLUSION

We have introduced an evolutionary generation of microwave line-segment circuits using the GA. The developed procedure optimizes a line-segment circuit with a variety of topology and ends up with a circuit that exceeds expectations. The procedure also guarantees the circuit not be larger than the size specified in advance. Some examples of unconventional specifications were tested to validate the procedure. It is found that the GA has a strong design capability for microwave line-segment circuits with specifications for which no traditional approach can be used.

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REFERENCES

- [1] J. H. Holland, *Adaptation in Natural and Artificial Systems*. Ann Arbor, MI: Univ. Michigan Press, 1975.
- [2] E. Michielssen, J. M. Sajer, and R. Mittra, "Design of multilayered FSS and wave guide filter using genetic algorithms," in *IEEE AP-S Int. Symp. Dig.*, 1993, pp. 1936-1939.
- [3] J. M. Johnson and Y. Rahmat-Samii, *A Novel Integration of Genetic Algorithms and Method of Moment (GA/MoM) for Antenna Design*. Reading, MA: Addison-Wesley, 1989.
- [4] Y. Rahmat-Samii and E. Michielssen, *Electromagnetic Optimization by Genetic Algorithms*. New York: Wiley, 1999.
- [5] J. R. Koza, F. H. Bennett, D. Andre, M. A. Keane, and F. Dunlap, "Automated synthesis of analog electrical circuits by mean of genetic programming," *IEEE Trans. Evol. Comput.*, vol. 1, pp. 109-128, July 1997.
- [6] A. John and R. H. Jansen, "Evolutionary generation of (M)MIC component shapes using 2.5D EM simulation and discrete genetic optimization," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1996, pp. 745-748.
- [7] K. C. Gupta, *Computer-Aided Design of Microwave Circuits*. Norwood, MA: Artech House, 1981.
- [8] J. A. Dobrowolski and W. Ostrowski, *Computer-Aided Analysis, Modeling and Design of Microwave Networks*. Norwood, MA: Artech House, 1996.



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